

# MOTOROLA

Motorola found Saber® to be a real time-saver for designing their complex read/write channel ICs.

# CORPORATION

Mike Pennell faced a challenge. His department was responsible for designing a new, high-speed PRML (Partial Response Maximum Likelihood) read/write channel IC for storage devices. In the highly competitive world of disk-drive controls, cutting time-to-market is a primary engineering goal. The pressure was on to get the new design completed as quickly as possible. The main obstacle? It was a very large mixed-signal chip with different design teams working on the individual blocks. Pennell had to put all the blocks together, check interoperability, fine tune performance, and optimize the feedback loops, while keeping all the different time constants straight. "That's when a high-level tool like Saber comes in very handy," said Pennell.

Pennell already had three years of successful experience with Analog's SaberDesigner™ product suite. One reason he chose Saber for this project was its ability to simulate both analog and digital circuits.

*Motorola's read/write channel ICs represent an engineering challenge for simulators.*

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Mike Pennell

Most of the IC's digital blocks had been simulated with Verilog-XL™, so he used Saber/Verilog to produce a unified simulation of the analog and digital portions working together.

The large amount of analog circuitry on the chip and the multiple feedback loops in the design were another reason to use Saber. Previously, simulations were not feasible on this type of design due to size and simulation time constraints. This meant that several time-consuming prototype steps were required before a production version of the design was available.

Pennell recalled using Saber on previous projects requiring high-level simulation. "We got our chips back and they worked very well, based on the top-level simulation. That was one of the keys to success. We just applied those techniques to the read/write channels."

Starting with a "bottom-up" modeling approach, Pennell developed behavioral models of the transistor-level blocks using Analog's MAST® Hardware Description Language. Circuit types included Viterbi detectors, automatic gain controls,



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charge pumps, D/A converters, biquad filters, programmable multipliers, programmable gain amplifiers and CML logic blocks. These models accurately reproduced the behavior of the transistor-level circuits. Assembling his behavioral blocks,

Pennell was able to simulate 90 percent of the chip with Saber/Verilog, representing all the critical blocks and feedback loops. Best of all, full chip simulations were completed in a matter of hours, whereas transistor level simulation took days for some of the chip sub-systems.

The simulation results indicated several problems including bus connectivity and stability problems in the complex feedback loops. "Once you have circuit-based models for all the blocks in the system and put them together, you can add connectivity checking to the separate blocks," said Pennell. "You can look for certain signals coming in and see if they are within expected levels. If they're not, you can conclude that this block is probably not connected properly. That's kind of an added bonus, doing signal and level checking between blocks. We actually found quite a few errors that way."

Most important of all, these problems were found *before* prototyping. Without the full-chip simulation, these problems probably would not have been detected until the prototype had been manufactured. "The old way of doing things was to simulate sub-systems, not the entire system together," said Pennell. "Basically, all our designers would work on their individual blocks and we'd put all the blocks together at the last minute, cross our fingers, and hope everything came out OK. Using Saber to simulate all the blocks is a new and much better approach for us."

When the first prototype came back from manufacturing, the portions of the IC that were simulated with Saber all worked correctly. "We saved a couple of masking turns," said Pennell. "That could be

three to six months — a *big* time-to-market advantage for an industry like ours!"

Pennell did have some problems getting his simulations to run successfully. "We had over 250 blocks and models operating simultaneously. When we first started out, we had some convergence problems. Ron Evans [Analogy's field applications engineer] helped us develop new methods to put all these blocks together. We now have a process that lets us link as many blocks as necessary, without any convergence problems."

Thanks to Mike Pennell's pioneering efforts, the benefits of using Saber have now spread to other engineering groups in Motorola and the company continues to discover new uses for Saber while constantly improving its critical time-to-market capabilities.



Mike Pennell was born and raised in Phoenix, Arizona. He earned his BSEE and MSEE at Arizona State University and is currently a PhD candidate in Electrical Engineering. After 11 years with Motorola, Mike has recently taken a job with Intel. His technical interests include low voltage analog circuits,

analog to digital converters, and mixed-signal simulation. Not a surprise from someone born in the year of the monkey.

This Motorola success story tied for third place in the 1997 Saber Success Award competition. Mike would like to acknowledge Bill Forni, IC designer at Motorola, for his valuable work on this project.

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